CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1   1.   A process of testing spacing of wiring in a circuit comprising:

2   forming a plurality of conductor rectangles representative of conductors of

3   said circuit;

4   forming minimum spacing rectangles around said conductor rectangles,

5   said minimum spacing rectangles being larger than respective ones of said

6   conductor rectangles;

7   identifying a possible error rectangle when a first conductor rectangle of

8   said conductor rectangles occupies a portion of a minimum spacing rectangle of a

9   second conductor rectangle of said conductor rectangles;

10   checking whether said possible error rectangle is a true error; and

11   reporting said true errors.

1   2.   The process in claim 1, wherein said checking comprises:

2   classifying said possible error rectangle as a possible diagonal error

3   rectangle or a possible non-diagonal error rectangle;

4   determining that said possible diagonal error rectangle is said not a true

5   error when at least two adjacent sides of said possible diagonal error rectangle

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6   which connect said first conductor and said second conductor are covered by a

7   third conductor of said conductors; and

8   determining that said possible non-diagonal error rectangle is not a true

9   error when said possible non-diagonal error rectangle is completely covered by said

10   third conductor.

1   3.   The process in claim 1, wherein said forming minimum spacing rectangles

2   comprises forming said minimum spacing rectangles to have sides which are a

3   minimum spacing design constraint distance from sides of respective ones of said

4   conductor rectangles.

1   4.   The process in claim 1, wherein said conductors are within a single net.

1   5.   The process in claim 1, wherein said circuit comprises a plurality of nets

2   and said process further includes checking for shorts between different ones of said

3   nets.

1   6.   The process in claim 1, further comprising dividing said possible error

2   rectangle into at least two possible error rectangles if said possible error rectangle

3   is partially covered by a third conductor of said conductors.

1   7.   A process of testing spacing of elements in a structure comprising:

2   forming a plurality of element rectangles representative of elements of said

3   structure;

4   forming minimum spacing rectangles around said element rectangles, said

5   minimum spacing rectangles being larger than respective ones of said element

6   rectangles;

7   identifying a possible error rectangle when a first element rectangle of said

8   element rectangles occupies a portion of a minimum spacing rectangle of a second

9   element rectangle of said element rectangles;

10   checking whether said possible error rectangle is a true error; and

11   reporting said true errors.

1   8.   The process in claim 7, wherein said checking comprises:

2   classifying said possible error rectangle as a possible diagonal error

3   rectangle or a possible non-diagonal error rectangle;

4   determining that said possible diagonal error rectangle is said not a true

5   error when at least two adjacent sides of said possible diagonal error rectangle

6   which connect said first element and said second element are covered by a third

7   element of said elements; and

8   determining that said possible non-diagonal error rectangle is not a true

9   error when said possible non-diagonal error rectangle is completely covered by said

10   third element.

1   9.   The process in claim 7, wherein said forming minimum spacing rectangles

2   comprises forming said minimum spacing rectangles to have sides which are a

3   minimum spacing design constraint distance from sides of respective ones of said

4   element rectangles.

1   10.   The process in claim 7, wherein said elements are within a single net.

1   11.   The process in claim 7, wherein said structure comprises a plurality of nets

2   and said process further includes checking for shorts between different ones of said

3   nets.

1   12.   The process in claim 7, further comprising dividing said possible error

2   rectangle into at least two possible error rectangles if said possible error rectangle

3   is partially covered by a third element of said elements.

1   13.   A computer system for testing spacing of wiring in a circuit comprising:

2   a unit for forming a plurality of conductor rectangles representative of conductors

3   of said circuit;

4   a unit for forming minimum spacing rectangles around said conductor

5   rectangles, said minimum spacing rectangles being larger than respective ones of

6·   said conductor rectangles;

7   a unit for identifying a possible error rectangle when a first conductor

8   rectangle of said conductor rectangles occupies a portion of a minimum spacing

9   rectangle of a second conductor rectangle of said conductor rectangles;

10   a unit for checking whether said possible error rectangle is a true error; and

11   a unit for reporting said true errors.

1   14.   The computer system in claim 13, wherein said unit for checking

2   comprises:

3   a unit for classifying said possible error rectangle as a possible diagonal

4   error rectangle or a possible non-diagonal error rectangle;

5   a unit for determining that said possible diagonal error rectangle is said not

6   a true error when at least two adjacent sides of said possible diagonal error

7   rectangle which connect said first conductor and said second conductor are covered

8   by a third conductor of said conductors; and

9   a unit for determining that said possible non-diagonal error rectangle is not

10   a true error when said possible non-diagonal error rectangle is completely covered

11   by said third conductor.

12   15.   The computer system in claim 13, wherein said unit for forming minimum

13   spacing rectangles comprises a unit for forming said minimum spacing rectangles

14   to have sides which are a minimum spacing design constraint distance from sides

15   of respective ones of said conductor rectangles.

1 16. The computer system in claim 13, wherein said conductors are within a

2 single net.

1 17. The computer system in claim 13, wherein said circuit comprises a plurality

2 of nets and said computer system further includes a unit for checking for shorts

3 between different ones of said nets.

1 18. The computer system in claim 13, further comprising a unit for dividing

2 said possible error rectangle into at least two possible error rectangle if said

3 possible error rectangle is partially covered by a third conductor of said conductors.

1 19. A computer program product comprising a program storage device readable

2 by a computer system tangibly embodying a program of instructions executed by

3 said computer system to perform a process for testing spacing of wiring in a circuit,

4 said process comprising:

5 forming a plurality of conductor rectangles representative of conductors of

6 said circuit;

7 forming minimum spacing rectangles around said conductor rectangles,

8 said minimum spacing rectangles being larger than respective ones of said

9 conductor rectangles;

10   identifying a possible error rectangle when a first conductor rectangle of

11   said conductor rectangles occupies a portion of a minimum spacing rectangle of a

12   second conductor rectangle of said conductor rectangles;

13   checking whether said possible error rectangle is a true error; and

14   reporting said true errors.

1   20.   The computer program product in claim 19, wherein said checking

2   comprises:

3   classifying said possible error rectangle as a possible diagonal error

4   rectangle or a possible non-diagonal error rectangle;

5   determining that said possible diagonal error rectangle is said not a true

6   error when at least two adjacent sides of said possible diagonal error rectangle

7   which connect said first conductor and said second conductor are covered by a

8   third conductor of said conductors; and

9   determining that said possible non-diagonal error rectangle is not a true

10   error when said possible non-diagonal error rectangle is completely covered by said

11   third conductor.

1   21.   The computer program product in claim 19, wherein said forming

2   minimum spacing rectangles comprises forming said minimum spacing rectangles

3   to have sides which are a minimum spacing design constraint distance from sides

4   of respective ones of said conductor rectangles.

1   22.   The computer program product in claim 19, wherein said conductors are

2   within a single net.

1   23.   The computer program product in claim 19, wherein said circuit comprises

2   a plurality of nets and said process further includes checking for shorts between

3   different ones of said nets.

1   24.   The computer program product in claim 19, said process further comprising

2   dividing said possible error rectangle into at least two possible error rectangle if

3   said possible error rectangle is partially covered by a third conductor of said

4   conductors.